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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,162	11/25/2003	Atsushi Kuwata	8001-1176	4322

466 7590 04/19/2007
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EXAMINER

SUN, SCOTT C

ART UNIT	PAPER NUMBER
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2182

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,162	KUWATA, ATSUSHI	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 December 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/27</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed 12/15/2006 has been noted and entered. Previous rejections under U.S.C. 112 are withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivard (PG Pub# US2004/0078508 A1) in view of Weber (US Patent #5,596,708) further in view of George et al (PG Pub #2003/0041215).
3. As per claim 1, Rivard discloses a disk array apparatus (figure 2) comprising a cache memory (data store 210) that temporarily stores data to be read from or written to

Art Unit: 2182

first and second disks (paragraphs 45, 48, 54-56); Examiner notes that Rivard teaches data store 210 holds read data, and WCC, which functions as a write cache and controller, can be integrated with the data store. Alternatively, WCC can be implemented to also have a read cache (paragraph 56).

Rivard further teaches a control unit (cache access concentrator 201, comprising WCC units) which transforms said data into a physical domain of said cache memory so as to associate said data with physical addresses (paragraphs 55, 58; 70); Examiner notes that Rivard teaches WCC uses a protocol such as SCSI or ATAPI for communication with the disks, in either case LBA (logical block address) of the data would be used. In order to read or write data to the physical disk, LBA is translated (transformed) into a corresponding physical disk block location, usually in terms of cylinder-head-sector. It would then allow the data to be written to the physical disks.

Although Rivard teaches write scheduling and a plurality of disks, Rivard does not teach explicitly generating check information. However, Weber teaches generating check information (parity data) on the basis of said data (column 8, lines 9-51).

Teachings of Rivard and Weber are from the same field of disk storage systems, and specifically of read/write performance.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Rivard and Weber by generating parity data in the storage system of Rivard for the benefit of protecting data from disk failures (Weber; column 1, lines 40-50).

Rivard and Weber combined do not disclose explicitly take precedence writing said data and check information over writing new data. However, George discloses a cache coherency method (write-through coherency, figure 4) in which writing of new data is delayed until more "senior" data is updated in coherent memory space (written to a physical location to which the cached data corresponds, paragraph 27).

Teachings of Rivard, Weber and George are from the same field of data input/output, and specially of command scheduling. Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Rivard and Weber, and further with George by using the cache coherency scheme in the combined system of Rivard and Weber for the benefit providing cache coherency.

4. As per claim 2, Rivard, Weber and George combined discloses the disk array apparatus as claimed in claim 1, and Rivard further teaches wherein said control unit releases the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed (paragraph 69).

5. As per claim 3, Rivard, Weber and George combined discloses the disk array apparatus as claimed in claim 1, and Rivard further teaches wherein said control unit comprises a plurality of control units (write cache controllers) which are physically independent of one another and wherein if a failure occurs in one control unit, another control unit takes over the preferential processing for the data associated with a physical address in the cache memory (paragraph 81).

Art Unit: 2182

6. As per claims 4-6, Rivard, Weber and George combined discloses the disk array apparatus as claimed in claim 1-3, wherein Rivard further teaches wherein said cache memory is a nonvolatile memory (paragraph 51, 52, 81). Examiner notes Rivard also teaches the use of NVRAM (non-volatile RAM) in prior art systems (paragraph 26).

7. As per claims 7-10, the examiner finds these claims contain substantially similar limitations as above rejected claims 1-6. Therefore, the same arguments are applied.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

TANH Q NGUYEN
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100


April 12, 2007